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FIG. 1

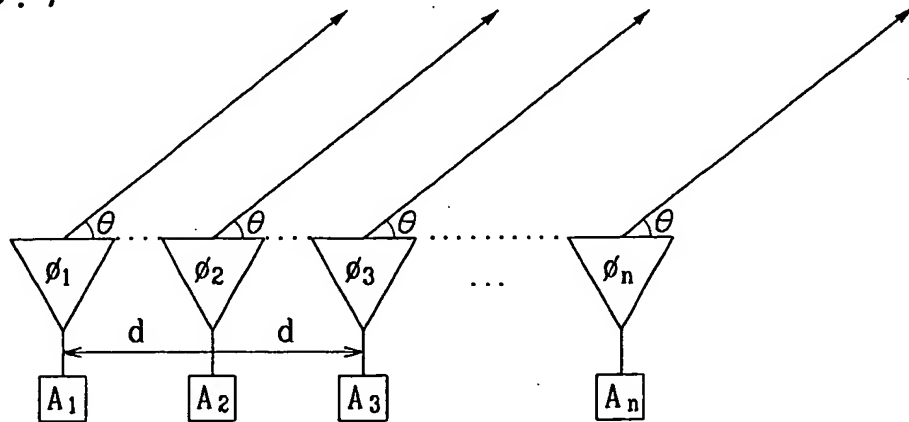


FIG. 2A

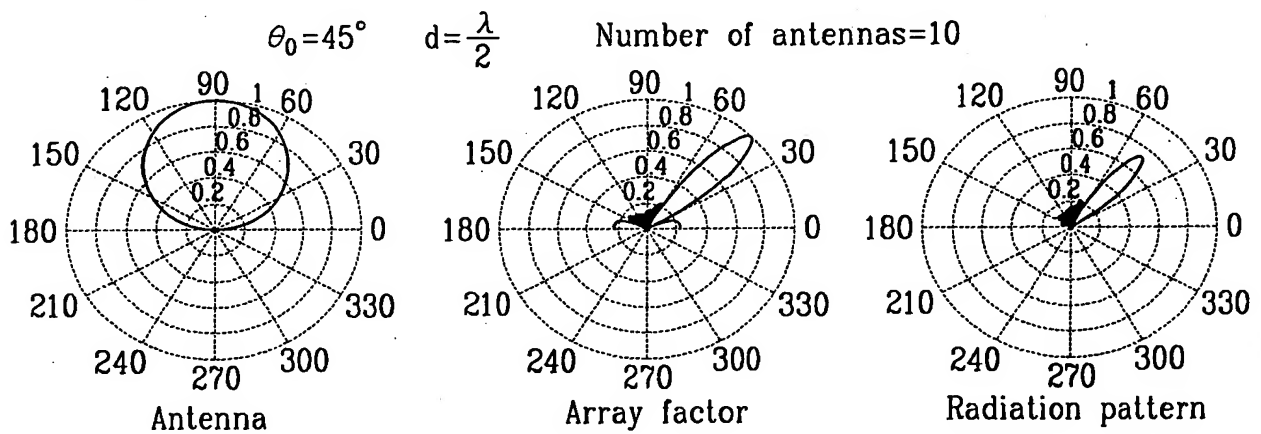
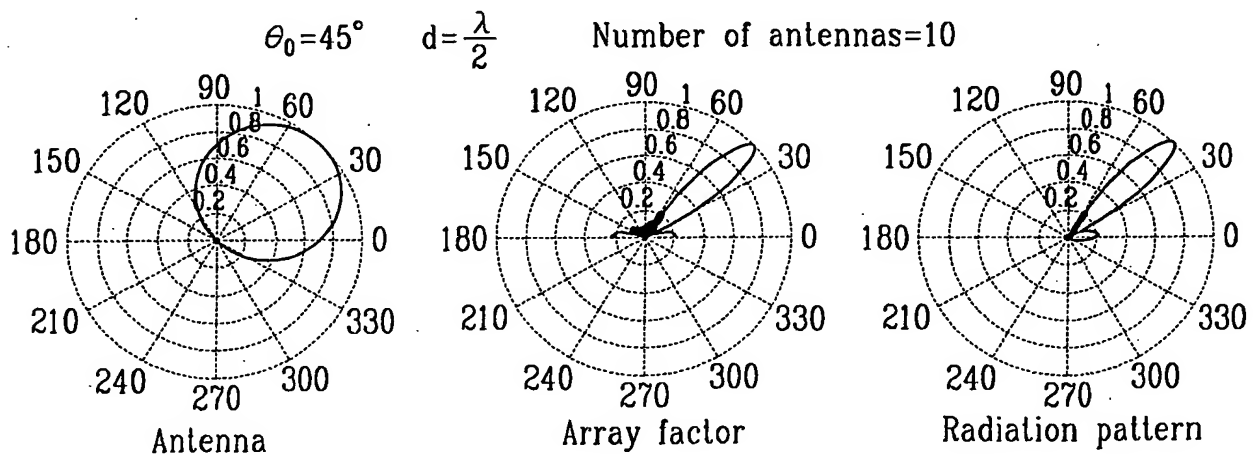


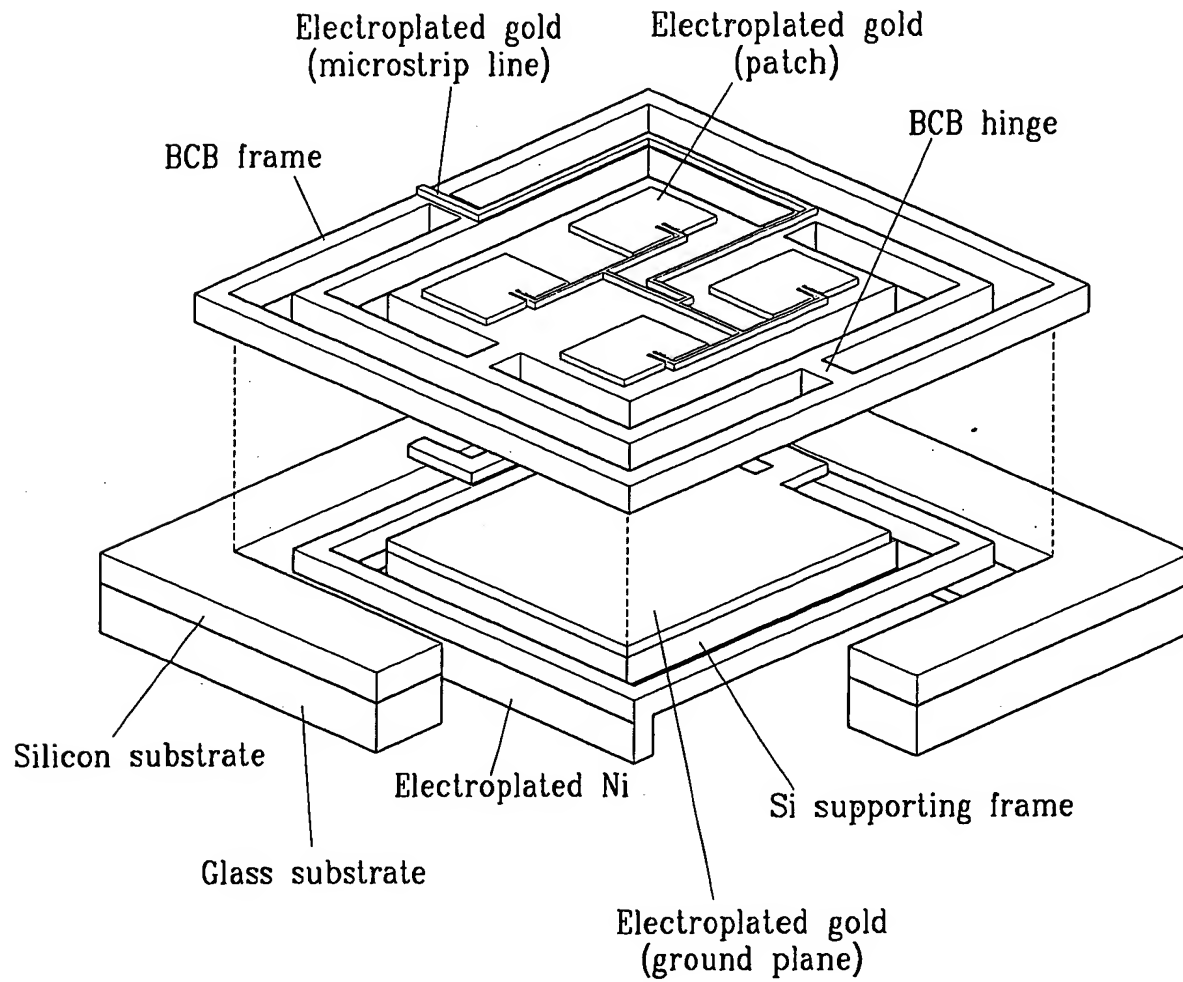
FIG. 2B



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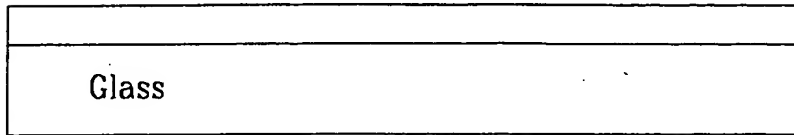
FIG. 3



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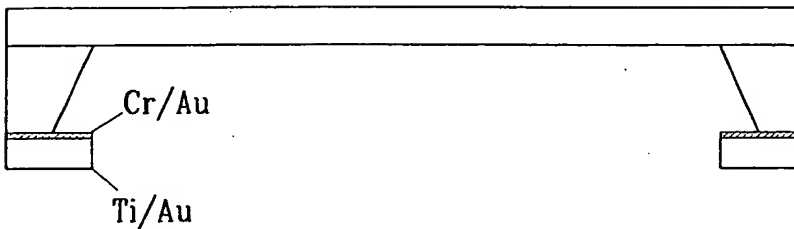
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FIG. 4A



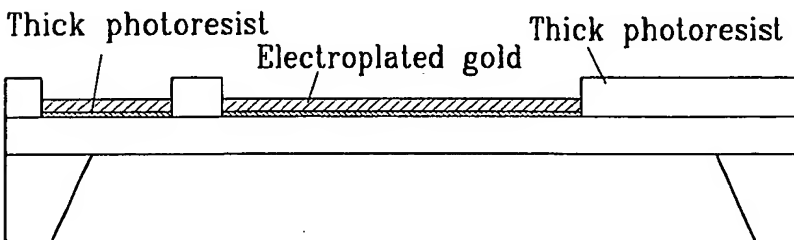
- \* Anodic bonding of glass & silicon
- \* Thinning of silicon using KOH
- \* CMP of silicon

FIG. 4B



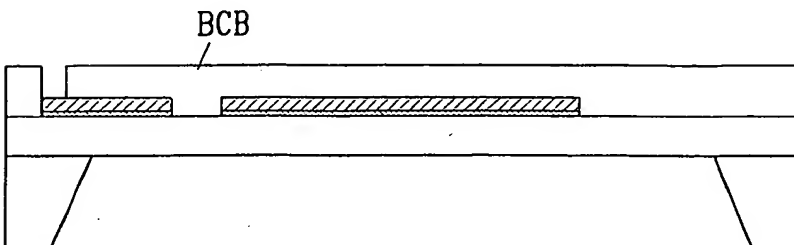
- \* Cr/Au deposition
- \* Photolithography #1
- \* Au/Cr etch
- \* Hardbake of photoresist
- \* Glass etching

FIG. 4C



- \* 1st seed layer deposition
- \* Photolithography #2
- \* Electroplating

FIG. 4D

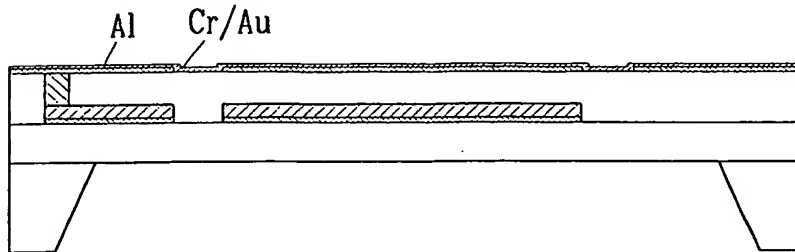


- \* PR strip
- \* Seed layer etching
- \* BCB coating & baking
- \* BCB patterning

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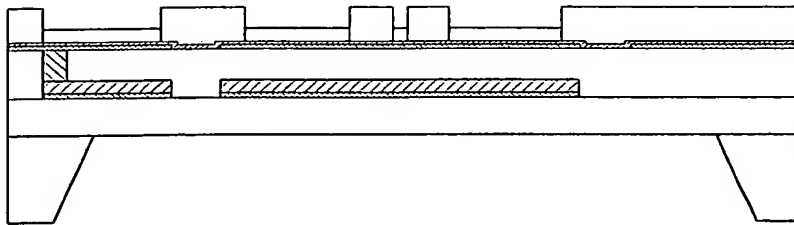
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FIG. 4E



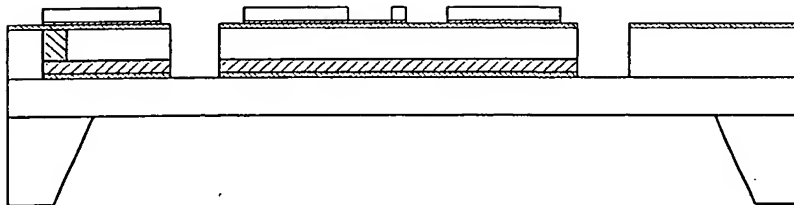
- \* Au electroplating (for via)
- \* Al mask deposition
- \* Photolithography #3
- \* Al etching
- \* 2nd seed layer deposition

FIG. 4F



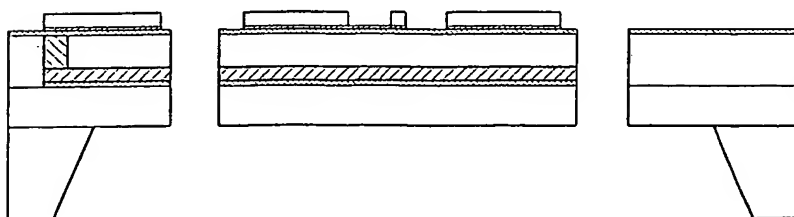
- \* Photolithography #4
- \* Au electroplating

FIG. 4G



- \* PR strip
- \* Seed layer etching
- \* RIE of BCB

FIG. 4H



- \* Silicon deep RIE

FIG. 5

